IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: To Be Assigned Examiner: To Be Assigned

In re PATENT APPLICATION of:

Applicant(s) : Toshio NAGATA

Appln. No. : To Be Assigned

Filed : June 27, 2003) INFORMATION) DISCLOSURE) STATEMENT

For : METHOD OF FABRICATING A

SEMICONDUCTOR DEVICE

INCLUDING A TUNNEL OXIDE FILM

Atty. Dkt. : MAE 286

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

This is an information disclosure statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97(b)(1).

Attached is a copy of a Japanese publication. Any relevance of the Japanese publication can be gleaned from the attached English-language Abstract. The document is listed on the attached Form PTO-1449.

Since this Information Disclosure Statement is being filed with the application, no certification or fee is required, and the requirements of 37 C.F.R. §§1.97 and 1.98 are deemed to be fully met as to the document submitted. Consideration of the submitted document is respectfully requested.

June 27, 2003

Date

Robert H. Berdo, Jr. (Reg. No. 3/8,075)

RABIN & BERDO, P.C. CUSTOMER NO. 23995

Respectfully submitted,

(202) 371-8976 (202) 408-0924 fax

RHB:tz

FEE ENCLOSED:\$ 790
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f t ur Deposit Account
N . 18-0002

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				Atty Docket	Applica	Application No. To Be Assigned		
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				Applicant Toshio NAGATA				
				June 27, 2003	To Be	To Be Assigned		
			U.S. F	PATENT DOCUMENTS				
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		Document Number	Date	Country	Class	Sub- Class	Trans- lation	
	АН	08-255905	10/01/96				Abstract	
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		OTHER (Including Au	thor, Title, Date, Pertinent Pages, et	c.)		<u> </u>	
James C.M. Hwang, "Relationship between gate lag, power drift, and power slump of pseudomorphic high electron mobility transistors", Solid-State Electronics 43 (1999), pp. 1325-1331								
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Examiner	1,			Date Considered				
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